TUNA NVM-H2 NVRAM Emulation Board

User Guide

Version 1.0
2014-11-19

Revision History

Date	Version	Revision
11/19/2014	1.0	Initial Release

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Overview

NVM-H2 Board Feature

XC7Z045-3FFG900 Zynq-7000 FPGA

- Dual ARM Cortex-A9 1GHz Core
- NEON DSP co-processor for each core
- 350K LCs

1GB DDR3 component memory on PS side
Two 128Mb Quad-SPI(QSPI) Flash Memories
SODIMM DDR3 Memory Slot
1 SD CARD connector
Dual PCIe Gen2 4-lane(x4) End-Points (Cabled PCIe Interface)
1 Gigabit Ethernet Interface
1 USB 2.0 (configurable to Host or Device)
JTAG and Debug Interface
1 USB-UART Port
1 ARM JTAG
1 PL JTAG
Status LEDs
Buttons and Tactile switches
Indicators and Switches LEDs and Tactile switches

Board Layout

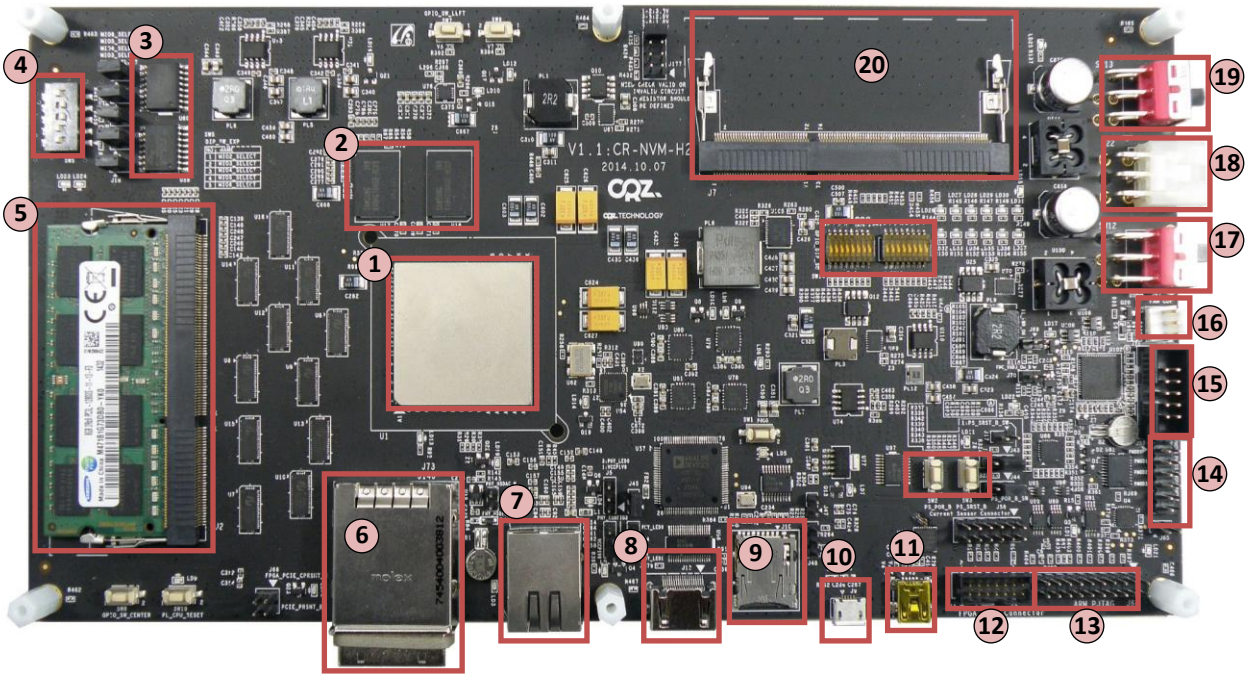

Table 1-1: NVM-H2 Board Components Descriptions

Number	Part number	Description
1	U1	XC7Z045-3FFG900 Xilinx Zynq-7000 SoC FPGA
2	U17,U18	DDR3 Component Memroy (PS), 1GB
3	U59, U60	128 Mb QSPI memory
4	SW5	Configuration mode select switch
5	J2	SODIMM DDR3 for PL
6	J73	External PCIe connector #0 (support endpoint and root complex)
7	J6	Gigabit Ethernet
8	J12	HDMI Video output
9	J10	Micro SD card connector
10	J9	Micro USB 2.0 ULTP
11	J14	USB to UART Mini-B connector
12	J1	14 pin JTAG connector
13	J64	20 pin ARM JTAG connector
14	J57	PMOD pin
15	J71	PMbus connector
16	J67	FAN connector
17	SW12	Board power switch
18	J22	6pin ATX power connector
19	SW13	SODIMM DDR3 power switch
20	J7	SODIMM Expansion for NADN and general purpose

Feature Descriptions

Detailed information for each feature is provided in this section.

DDR3 Component Memory (PS)

The 1 GB, 32-bit wide DDR3 component memory system is comprised of two 4 Gbit x16 SDRAMs (Samsung K4B2G1646C) at U17, U18. This memory system is connected to the XC7Z045 AP SoC Processing System (PS) memory interface bank 502. The DDR3 0.75V VTT termination voltage is sourced from linear regulator U76. The connections between the DDR3 component memory and XC7Z045 AP SoC bank 502 are listed in Table 1-2.

Table 1-2: DDR3 Component Memory connections to the XC7Z045 AP Soc

XC7Z045 Pin	Net Name	Component Memory		
		Pin Number	Pin Name	Ref. Des
F25	PS_DDR3_RESET_B	T2	RESETn	U17/U18
E25	PS_DDR3_DQ1	F7	DQL1	U17
A25	PS_DDR3_DQ0	E3	DQL0	U17
D25	PS_DDR3_DQ3	F8	DQL3	U17
B27	PS_DDR3_DM0	E7	DML	U17
C27	PS_DDR3_DQ2	F2	DQL2	U17
B26	PS_DDR3_DQS0_N	G3	DQSLn	U17
C26	PS_DDR3_DQS0_P	F3	DQSL	U17
E26	PS_DDR3_DQ5	H8	DQL5	U17
B25	PS_DDR3_DQ4	H3	DQL4	U17
E27	PS_DDR3_DQ7	H7	DQL7	U17
D26	PS_DDR3_DQ6	G2	DQL6	U17
A27	PS_DDR3_DQ9	C3	DQU1	U17
A29	PS_DDR3_DQ8	D7	DQU0	U17
A28	PS_DDR3_DQ11	C2	DQU3	U17
A30	PS_DDR3_DQ10	C8	DQU2	U17
B30	PS_DDR3_DM1	D3	DMU	U17
B29	PS_DDR3_DQS1_N	B7	DQSUn	U17
C29	PS_DDR3_DQS1_P	C7	DQSU	U17
D30	PS_DDR3_DQ13	A2	DQU5	U17
C28	PS_DDR3_DQ12	A7	DQU4	U17

D29	PS_DDR3_DQ15	A3	DQU7	U17
D28	PS_DDR3_DQ14	B8	DQU6	U17
H23	PS_DDR3_A13	T3	A13	U17/U18
J24	PS_DDR3_A14	T7	A14/NC	U17/U18
H24	PS_DDR3_A11	R7	A11	U17/U18
K23	PS_DDR3_A12	N7	A12/BCn	U17/U18
J23	PS_DDR3_A9	R3	A9	U17/U18
G26	PS_DDR3_A10	L7	A10/AP	U17/U18
K22	PS_DDR3_A7	R2	A7	U17/U18
F27	PS_DDR3_A8	T8	A8	U17/U18
G24	PS_DDR3_A5	P2	A5	U17/U18
H26	PS_DDR3_A6	R8	A6	U17/U18
G25	PS_DDR3_A3	N2	A3	U17/U18
J26	PS_DDR3_A4	P8	A4	U17/U18
K25	PS_DDR3_CLK_P	J7	CK	U17/U18
J25	PS_DDR3_CLK_N	K7	CKn	U17/U18
L27	PS_DDR3_A2	P3	A2	U17/U18
K26	PS_DDR3_A1	P7	A1	U17/U18
L25	PS_DDR3_A0	N3	A0	U17/U18
M25	PS_DDR3_BA2	M3	BA2	U17/U18
M26	PS_DDR3_BA1	N8	BA1	U17/U18
M27	PS_DDR3_BA0	M2	BA0	U17/U18
L23	PS_DDR3_ODT	K1	ODT	U17/U18
N22	PS_DDR3_CS_B	L2	CSn	U17/U18
M22	PS_DDR3_CKE	K9	CKE	U17/U18
N23	PS_DDR3_WE_B	L3	WEn	U17/U18
M24	PS_DDR3_CAS_B	K3	CASn	U17/U18
N24	PS_DDR3_RAS_B	J3	RASn	U17/U18
H27	PS_DDR3_DQ16	E3	DQL0	U18
G27	PS_DDR3_DQ17	F7	DQL1	U18
H28	PS_DDR3_DQ18	F2	DQL2	U18
E28	PS_DDR3_DQ19	F8	DQL3	U18
H29	PS_DDR3_DM2	E7	DML	U18
G29	PS_DDR3_DQS2_P	F3	DQSL	U18
F29	PS_DDR3_DQS2_N	G3	DQSLn	U18
E30	PS_DDR3_DQ20	H3	DQL4	U18

F28	PS_DDR3_DQ21	H8	DQL5	U18
G30	PS_DDR3_DQ22	G2	DQL6	U18
F30	PS_DDR3_DQ23	H7	DQL7	U18
J29	PS_DDR3_DQ24	D7	DQU0	U18
K27	PS_DDR3_DQ25	C3	DQU1	U18
J30	PS_DDR3_DQ26	C8	DQU2	U18
J28	PS_DDR3_DQ27	C2	DQU3	U18
K28	PS_DDR3_DM3	D3	DMU	U18
L28	PS_DDR3_DQS3_P	C7	DQSU	U18
L29	PS_DDR3_DQS3_N	B7	DQSUn	U18
K30	PS_DDR3_DQ28	A7	DQU4	U18
M29	PS_DDR3_DQ29	A2	DQU5	U18
L30	PS_DDR3_DQ30	B8	DQU6	U18
M30	PS_DDR3_DQ31	A3	DQU7	U18

Quad-SPI Flash Memory

The Quad-SPI flash memory located at U59 and U60 provides 2 x 128 Mb of nonvolatile storage that can be used for configuration and data storage.

- Part number: S25FL128SAGMFI001 (Spansion)
- Supply voltage: 1.8V
- Datapath width: 4 bits
- Data rate: Various depending on Single/Dual/Quad mode

The connections between the SPI flash memory and the XC7Z045 AP SoC are listed in Table 1-3.

Table 1-3: Quad-SPI Flash Memory connection to the XC7Z045 AP SoC

XC7Z045 (U1)			**Schematic Net Name**	**Quad-SPI Flash memory**		**QSPI Device**	**MIO Select Header**
Pin name	Bank	Pin Number		Pin number	Pin name	Ref.Des	
PS_MIO1	500	D23	QSPI0_CS_B	7	CS_B	U59	N/A
PS_MIO6	500	D24	QSPI0_CLK	16	SCK	U59	J20.1
PS_MIO2	500	F23	QSPI0_IO0	15	SI_IO0	U59	J18.1
PS_MIO3	500	C23	QSPI0_IO1	8	SO_IO1	U59	J19.1
PS_MIO4	500	E23	QSPI0_IO2	9	WP_B_IO2	U59	J21.1
PS_MIO5	500	C24	QSPI0_IO3	1	HOLD_B_IO3	U59	J22.1
PS_MIO0	500	F24	QSPI1_CS_B	7	CS_B	U60	N/A
PS_MIO9	500	A24	QSPI1_CLK	16	SCK	U60	N/A
PS_MIO10	500	E22	QSPI1_IO0	15	SI_IO0	U60	N/A
PS_MIO11	500	A23	QSPI1_IO1	8	SO_IO1	U60	N/A
PS_MIO12	500	E21	QSPI1_IO2	9	WP_B_IO2	U60	N/A
PS_MIO13	500	F22	QSPI1_IO3	1	HOLD_B_IO3	U60	N/A

USB 2.0 ULPI Transceiver

The NVM-H2 board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI Transceiver at U58 to support a USB connection to the host computer. The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device which drives the physical USB bus. Use of the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.
The USB3320 is clocked by a 24 MHz crystal. Consult the SMSC USB3320 data sheet for clocking mode details.
The interface to the USB3320 transceiver is implemented through the IP in the XC7Z045 AP SoC Processor System.

Table 1-4 describes the jumper settings for the USB 2.0 circuit.

Header	Function	Shunt Position
J47	Host/OTG or device	Shunt ON(1) = Host or OTG mode Shunt OFF = Device mode
J48	RVBUS select	Position 1–2 = Device mode (10 KΩ) Position 2–3(1) = Host or OTG mode (1 KΩ)

Note:
1. Default shunt position

The connections between the USB Type-A connector at J9 and the PHY at U58 are listed in Table 1-5. USB Connector Pin Assignment and Signal Definitions Between J9 and U58

Header		Net Name	Description	USB3320 Pin
Pin	Name			
1	VBUS	USB_VBUS_SEL	+5V from host system	22
2	D_N	USB_D_N	Bidirectional differential serial data (N-side)	19
3	D_P	USB_D_P	Bidirectional differential serial data (P-side)	18
4	GND	GND	Signal ground	33

The connections between the USB 2.0 PHY at U58 and the XC7Z045 AP SoC are listed in Table 1-6.

Table 1-6. USB 2.0 ULPI Transceiver Connections to the XC7Z045 AP SoC

XC7Z045			Schematic Net Name	USB3320 Pin
Pin NAME	Bank	Pin Number		
PS_MIO36	501	H17	USB_CLKOUT	1
PS_MIO31	501	H21	USB_NXT	2
PS_MIO32	501	K17	USB_DATA0	3

PS_MIO33	501	G22	USB_DATA1	4
PS_MIO34	501	K18	USB_DATA2	5
PS_MIO35	501	G21	USB_DATA3	6
PS_MIO28	501	L17	USB_DATA4	7
PS_MIO37	501	B21	USB_DATA5	9
PS_MIO38	501	A20	USB_DATA6	10
PS_MIO39	501	F18	USB_DATA7	13
PS_MIO30	501	L18	USB_STP	29
PS_MIO29	501	H22	USB_DIR	31
PS_MIO7	500	B24	USB_RESET_B_AND	27

SD Card Interface

The NVM-H2 board includes a secure digital input/output (SDIO) interface to provide user-logic access to general purpose nonvolatile SDIO memory cards and peripherals. Information for the SD I/O card specification can be found at the SanDisk and SD card websites.
The SDIO signals are connected to XC7Z045 AP SoC PS bank 501 which has its VCCMIO set to 1.8V. A MAX13035E high-speed logic-level translator (U5) is used between XC7Z045 AP SoC 1.8V PS bank 501 and the 3.3V SD card connector (J10).

Table 1-7 lists the SD card interface connections to the XC7Z045 AP SoC

XC7Z045			Schematic Net Name	Level Shifter		SDIO Connector	
Pin NAME	Bank	Pin Number		1.8V Side Pin	3.3V Side Pin	Pin Number	Pin Name
PS_MIO15	500	C22	SDIO_SDWP	N/A	N/A	11	PROTECT
PS_MIO14	500	B22	SDIO_SDDET	N/A	N/A	10	DETECT
PS_MIO41	501	J18	SDIO_CMD_LS	10	8	2	CMD
PS_MIO40	501	B20	SDIO_CLK_LS	12	14	5	CLK
PS_MIO44	501	E20	SDIO_DAT2_LS	4	6	9	DAT2
PS_MIO43	501	E18	SDIO_DAT1_LS	3	5	8	DAT1
PS_MIO42	501	D20	SDIO_DAT0_LS	1	15	7	DAT0
PS_MIO45	501	H18	SDIO_CD_DAT3_LS	9	7	1	CD_DAT3

Clock Generation

The NVM-H2 board provides four clock sources for the XC7Z045 AP SoC.
Table 1-9 lists the source devices for each clock.
Table 1-9. Clock Sources

Clock Name	Clock Source	Description
System Clock	U61	SiT9102 2.5V LVDS 200 MHz fixed-frequency oscillator (SiTime).
User Clock	U62	Si570 3.3V LVDS I2C programmable oscillator, 156.250 MHz default(Silicon Labs).
PS Clock	U63	SIT8103 1.8V single-ended CMOS 33.3333 MHz fixed frequency oscillator (SiTime).
Jitter Attenuated Clock	U54	Si5324C LVDS precision clock multiplier/jitter attenuator (Silicon Labs).

Table 1-10 lists the pin-to-pin connections from each clock source to the XC7Z045 AP SoC.
Table 1-10. Clock Connections, Source to XC7Z045 AP SoC

Clock Source Pin	Net Name	XC7Z045 Pin
U61.4	SYSCLK_P	AG17
U61.5	SYSCLK_N	AG16
U62.4	USRCLK_P	AF14
U62.5	USRCLK_N	AG14
U63.3	PS_CLK	A22
U54.28	SI5324_OUT_P	AC8
U54.29	SI5324_OUT_N	AC7

GTX Transceivers

The NVM-H2 board provides access to 16 GTX transceivers:
• Four of the GTX transceivers are wired to the External PCI Express x4 endpoint edge connector (J73) fingers

The GTX transceivers in Zynq-7000 series AP SoCs are grouped into four channels described as Quads. The reference clock for a Quad can be sourced from the Quad above or Quad below the GTX Quad of interest. There are four GTX Quads on the NVM-H2 board with connectivity as shown here:
• Quad 109: not connected
• Quad 110: not connected
• Quad 111: not connected
• Quad 112:
    ° MGTREFCLK0 – PCIE1_CLK_Q0 PCIE Reference clock
    ° MGTREFCLK1 - not connected
    ° Contains 4 GTX transceivers allocated to PCIE1[0:3]

Table 1-11 lists the GTX Banks 112 interface connections between the AP SoC U1 and External PCIE Connector.

Table 1-11. AP SoC GTZ Bank 112 Interface Connections

Transceiver Bank	FPGA Pin Number	Schematic Net Name	Connected Pin	Connected Device
GTX_BANK_112	T2	PCIE_TX3_P	A11	External PCIE Connector
	T1	PCIE_TX3N	A12	
	V6	PCIE_RX3_P	B11	
	V5	PCIE_RX3_N	B12	
	R4	PCIE_TX2P	A8	
	R3	PCIE_TX2N	A9	
	U4	PCIE_RX2_P	B8	
	U3	PCIE_RX2_N	B9	
	P2	PCIE_TX1_P	A5	
	P1	PCIE_TX1_N	A6	
	T6	PCIE_RX1_P	B5	
	T5	PCIE_RX1_N	B6	
	N4	PCIE_TX0_P	A2	
	N3	PCIE_TX0_N	A3	
	P6	PCIE_RX0_P	B2	
	P5	PCIE_RX0_N	B3	

	N8	PCIE_CLK_Q0P	A14	
	N7	PCIE_CLK_Q0N	A15	
	R8	NC		
	R7	NC		

External PCI Express Endpoint Connectivity

The 8-lane External PCI Express connector performs data transfers at the rate of 2.5 GT/s for a Gen1 application and 5.0 GT/s for a Gen2 application. The PCIe transmit and receive signal data paths have a characteristic impedance of 85Ω ±10%. The PCIe clock is routed as a 100Ω differential pair.

The XC7Z045-2FFG900C AP SoC (-3 speed grade) included with the NVM-H2 board supports up to 1ea Gen2 x4. The PCIe clock is input from the edge connector. It is AC coupled to the AP SoC through the MGTREFCLK0 pins of Quad 112. PCIE_CLK_Q0_P is connected to AP SoC U1 pin N8, and the _N net is connected to pin N7.

USB to UART Bridge

The NVM-H2 board contains a Silicon Labs CP2103GM USB-to-UART bridge device (U82) which allows a connection to a host computer with a USB port. The CP2103GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the NVM-H2 board.

The CP2013GM TX and RX pins are wired to the UART_1 IP block within the XC7Z045 AP SoC PS I/O Peripherals set. The XC7Z045 AP SoC supports the USB-to-UART bridge using two signal pins: Transmit (TX) and Receive (RX).

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2103GM USB-to-UART bridge to appear as a COM port to communications application software (for example, TeraTerm or HyperTerm) that runs on the host computer. The VCP device drivers must be installed on the host PC prior to establishing communications with the NVM-H2 board.

The USB Connector pin assignments and signal definitions between J14 and U82 are listed in Table 1-12.

Table 1-12. USB Connector J14 Pin Assignments and Signal Definitions

USB Connector		Net Name	Description	CP2103GM	
Pin	Name			Pin	Name
1	VBUS	USB_UART_VBUS	+5V VBUS POWERED	7	REGIN
				8	VBUS
2	D_N	USB_UART_D_N	Bidirectional differential serial data (N-side)	4	D-
3	D_P	USB_UART_D_P	Bidirectional differential serial data (P-side)	3	D+
5	GND	USB_UART_GND	Signal ground	2	GND1
				29	CNR_GND

Table 1-13 lists the USB connections between the XC7Z045 AP SoC PS Bank 501 and the CP2103 UART bridge.

Table 1-13. XC7Z045 AP SoC CP2103 Connections

XC7Z045 AP SoC						Schematic Net Name	CP2103GM Device		
Pin Name	Bank	Pin	Fucntion	Direction	IOSTANDARD		Pin	Function	Direction
PS_MIO48	501	C19	TX	Output	LVCMOS18	USB_UART_RX	24	RXD	Input
PS_MIO49	501	D18	RX	Input	LVCMOS18	USB_UART_TX	25	TXD	Output

Refer to the Silicon Labs website for technical information on the CP2103GM and the VCP Drivers.

For additional information on the Zynq-7000 AP SoC device UART controller, see Zynq-7000 All Programmable SoC Overview (DS190) and Zynq-7000 All Programmable SoC Technical Reference Manual (UG585).